

CLAIMS

What is claimed is:

1. A computer system, comprising:
 - a host processor;
 - an input device coupled to said host processor; and
 - a bridge coupled to said host processor, said bridge couples together a first bus and a second bus;wherein said bridge drives a signal on the first bus if said signal is being actively driven by a device coupled to the second bus, but not if said signal is only being actively driven by a device coupled to the first bus.
2. The computer system of claim 1 wherein said bridge includes a comparator to drive said signal, said comparator has one input coupled to a threshold and another input coupled to the signal from both the first and the second bus.
3. The computer system of claim 2 wherein said threshold is set at a level between the level at which a device on the first bus would cause said signal to be driven to and the level at which a device on the second bus would cause said signal to be driven to.
4. The computer system of claim 2 wherein said bridge includes a comparator for each signal on each of said first and second buses, each comparator used to drive a signal on one of the buses if such signal is being actively driven by a device coupled to the other of said buses, but not if the

1 10. The bridge device of claim 9 wherein each comparator causes a signal on one of the buses
2 to be driven if that signal is being actively driven by a bus device coupled to the other of said
3 buses, but not if the signal is only being actively driven by a bus device coupled to the bus having
4 the signal being driven by the comparator.

1 11. The bridge device of claim 9 wherein said threshold of each comparator is set at a level
2 between the level at which a bus device on the first bus would cause said signal to be driven to and
3 the level at which a bus device on the second bus would cause said signal to be driven to.

1 12. The bridge device of claim 9 wherein the bridge includes a logic gate coupled to each
2 comparator, said logic gate capable of being disabled by an enable signal to disable the bridging
3 function of the bridge.

1 13. The bridge device of claim 9 wherein said first and second buses comprise buses on which
2 more than one device can actively and concurrently drive a signal on the buses.

1 14. The bridge device of claim 9 wherein said first and second buses comprise I²C buses.

1 15. A method of bridging two buses together, comprising:

2 (a) comparing the voltage level of a bus signal coupled to both buses to a threshold level;

3 (b) determining which bus is actively driving said bus signal; and

4 (c) asserting said bus signal on one of the buses if such signal is being actively driven by
5 the other of said buses.

1 16. The method of claim 15 wherein said buses include a plurality of signals and (a), (b) and
2 (c) are performed for each of said signals.

1 17. The method of claim 15 wherein said buses comprise I²C buses.

1 18. A computer system, comprising:

2 a host processor; and

3 a bridge coupled to said host processor, said bridge couples together a first bus and a
second bus, said bridge includes a means for determining whether a bus is actively
asserting a bus signal and driving said signal on the other of said buses.

4 19. A bridge interconnecting two buses including a plurality of cross-coupled comparator units
that determine which bus is actively driving a bus signal or whether both buses are actively driving
said bus signal.

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